**Face-To-Face Student/Supervisor Meeting Record**

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| **Project Title:** | Design and Implementation of a Multi-core Processor using FPGA | **Photo:** |  |
| **Student Name:** | Matteo Bovino | **Student ID:** | 8671055 |
| **Supervisor:** | Dr Server Kasap | **Student UID:** |  |
| **Supervisor UID:** |  | **Department:** | AAEEE |
| **Course Code:** | Electrical and Electronic Engineering | **Module Code:** | 306AAE |
| **Date Today:** | 19/02/2021 | **Time:** | 02:00 PM |

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| **Current Progress and Issues:** | |
| *In this meeting I have showed all the progress made with regards to the one-core and dual-core design. At the moment, the one-core design is capable of executing the Fibonacci test sequence, placing the correct result in the given memory address after 4100 ns. Significant development has also been reached with respect to the dual-core system, I have duplicated the main pipeline with some slight adjustments in order to execute two instructions in one clock cycle. The critical issue is the cache coherency protocol which needs to be altered in order to allow safe and reliable data transfers between the caches. The MESI based snooping caches have already been coded in SystemVerilog but the bus system used to transfer the data needs to be re-analysed so that both cores can share information in a consistent manner.* | |
| **Agreed Key Action Points:** | |
| *While discussing the current design we also set targets for the next meeting. The agreed goal is to adjust the coherency protocol so that both cores can work effectively on a given test program. The program which I plan on using for the dual-core processor is a parallel program which is highlighted in the “Design and Implementation of a Multicore Processor Using FPGA” book. In the upcoming two weeks all the essential components of the design should be up and running and a simulation with the correct results will be provided during the meeting.* | |
| **Date and Time of next meeting:** | 02:00 PM 5/03/2021 |

*Signatures of those present:*

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| **Supervisor:** |  |
| **Student: Matteo Bovino** |  |